UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,958,712 B1
DATED : October 25, 2005
INVENTOR(S) : Rajaram Subramoniam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,
Line 38, after "signal" delete "1", and insert -- I, --.

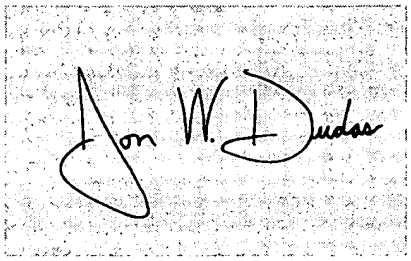
Column 4,
Line 33, after "reaches" delete "SF-I" and insert -- SF-1 --.
Lines 40-48, delete "Code logic circuit 404 is arranged to evaluate the number of valid bits in the code number according to the SF. The number of valid bits (N) is equal to $\log_2$ (SF). For example, an SF of 2 corresponds to one valid bit, an SF of 4 corresponds to two valid bits, and an SF of 8 corresponds to three valid bits. The most significant valid bit from the code number signal (code) is moved to the bit 7 position of the right justified code number signal (rjcode). All bits other than the N most significant bits are adjusted to zero." and insert the same in Col. 4, line 39, after "(code).".

Column 5,
Line 6, delete "SF-I" and insert -- SF-1 --.

Column 9,
Line 63, delete "fist" and insert -- first --.

Signed and Sealed this

Fourteenth Day of March, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office